

# Contents

---

---

## About This Book

The MindShare Architecture Series .....	1
Cautionary Note .....	2
Specifications This Book is Based On .....	3
Organization of This Book .....	3
Part One: Overview of USB 2.0.....	3
Part Two: Low- & Full-Speed Device Operation .....	4
Part III: High-Speed Device Operation.....	5
Part IV: USB 2.0 Hub Operation with LS/FS/HS Devices .....	5
Part VI: USB Software Overview.....	6
Appendices .....	7
Who Should Read this Book .....	7
Prerequisite Knowledge .....	7
Documentation Conventions.....	8
Hexadecimal Notation .....	8
Binary Notation.....	8
Decimal Notation .....	8
Bits Versus Byte Notation.....	8
Identification of Bit Fields (logical groups of bits or signals) .....	9
Visit Our Web Page .....	9
We Want Your Feedback.....	9

---

## Part One Overview of USB 2.0

---

### Chapter 1: Design Goals of USB

Shortcomings of the Original PC I/O Paradigm .....	13
Limited System Resources .....	14
Interrupts .....	15
I/O Addresses.....	16
Non-shareable Interfaces .....	16
End User Concerns .....	16
Cable Crazed .....	17
Installation and Configuration of Expansion Cards .....	17
No Hot Attachment of Peripherals .....	17
Cost .....	18
The USB Paradigm.....	18
Enhanced System Performance.....	19
Hot Plug and Play Support .....	20

# Contents

---

Expandability.....	20
Legacy Hardware/Software Support .....	20
Low Cost .....	21
Summary of Key USB Features.....	23
<b>How to Get the USB Specifications.....</b>	<b>24</b>

---

## Chapter 2: The Big Picture

<b>Overview.....</b>	<b>25</b>
<b>USB 1.x Systems and Devices.....</b>	<b>28</b>
Low-Speed and Full-Speed Devices.....	28
How Transactions Are Generated.....	30
What the Descriptors Contain.....	30
How the Transfer Descriptors Are Fetched .....	30
Frame Generation .....	33
Sharing the Bus.....	34
Bandwidth Consideration Summary .....	34
<b>2.0 Systems and Devices .....</b>	<b>37</b>
Low-Speed and Full-Speed Devices in a 2.0 System .....	38
Example 2.0 Host Controller Support for LS/FS Devices .....	40
High-Speed Devices in a 2.0 System .....	41
High-Speed Devices Attached to 1.x Ports .....	41
High-Speed Transactions and Microframe Generation .....	42
High-Speed Bandwidth Summary .....	42
<b>The Players .....</b>	<b>44</b>
USB Client Drivers.....	45
USB Bus Driver.....	46
USB Host Controller Driver .....	46
USB Host Controller/Root Hub .....	47
The Host Controller .....	47
The Root Hub .....	48
USB Hubs .....	49
Hub Controller .....	51
Hub Repeater.....	52
Hub's Role in Configuration .....	53
USB Devices .....	53
High-Speed Devices .....	53
Full-Speed Devices .....	53
Low-Speed Devices .....	53
<b>USB Communications Model.....</b>	<b>54</b>
Communications Flow .....	54
Transfers, IRPs, Frames, and Packets.....	55
Transfers.....	55

# Contents

---

The USB Driver, IRPs, and Frames .....	57
The Host Controller Driver and Transactions.....	59
The Host Controller and Packets.....	60
<b>Device Framework (how devices present themselves to software).....</b>	<b>60</b>
Device Descriptors.....	60
Device Framework.....	63
USB Bus Interface Layer .....	63
USB Device Layer .....	64
Function Layer .....	65
<b>USB Peripheral Connection .....</b>	<b>66</b>
Full-Speed Hubs.....	66
High-Speed Hubs.....	67
High-Speed Devices .....	67
Low- and Full-Speed Devices .....	67
<b>Topology .....</b>	<b>67</b>

---

## Chapter 3: Cables and Connectors

<b>The Connectors.....</b>	<b>69</b>
Series A Connectors.....	71
Series B Connectors.....	71
<b>Cables .....</b>	<b>71</b>
Low-Speed Cables.....	72
Full- and High-Speed Cables .....	73
Cable Power .....	74
<b>Electrical and Mechanical Specifications.....</b>	<b>74</b>

---

## Chapter 4: USB Cable Power Distribution

<b>USB Power.....</b>	<b>75</b>
<b>Hubs.....</b>	<b>76</b>
Current Budget.....	76
Over-Current Protection .....	78
Voltage Drop Budget.....	78
Power Switching .....	79
<b>Bus-Powered Hubs .....</b>	<b>80</b>
Power During Hub Configuration .....	80
Bus-Powered Hub Attached to 500ma Port .....	80
Bus-Powered Hub Attached to 100ma Port .....	80
Bus-Powered Hub Attached to Port with >100ma but <500ma .....	81
Current Limiting .....	81
<b>Bus-Powered Devices .....</b>	<b>82</b>
Low-Power Devices .....	82

# Contents

---

High-Power Devices .....	83
Power During Configuration .....	83
Insufficient Port Power .....	84
<b>Self-Powered Hubs .....</b>	<b>86</b>
Power During Configuration .....	87
Locally Powered Bus Interface .....	87
Hybrid Powered Device .....	87
Current Limiting .....	88
<b>Self-Powered Devices .....</b>	<b>89</b>
Power During Configuration .....	89
Locally Powered Bus Interface .....	89
Hybrid Powered Device .....	89

---

## Part Two Low- & Full-Speed Device Operation

---

### Chapter 5: LS/FS Signaling Environment

<b>Overview.....</b>	<b>93</b>
<b>Detecting Device Attachment and Speed Detect.....</b>	<b>94</b>
Full-Speed Device Connect.....	98
Low-Speed Device Connect.....	100
Detecting Device Disconnect.....	101
<b>Bus Idle .....</b>	<b>102</b>
<b>Device RESET .....</b>	<b>103</b>
<b>Differential Signaling .....</b>	<b>104</b>
Differential Drivers.....	106
Full-Speed Drivers .....	106
Low-Speed Drivers .....	108
Hub Driver Characteristics.....	109
Differential Receivers .....	109
Start of Packet (SOP).....	109
End of Packet (EOP) .....	110
Single-Ended Receivers.....	110
<b>NRZI Encoding .....</b>	<b>111</b>
<b>Bit Stuffing .....</b>	<b>112</b>
<b>Summary of USB Signaling States .....</b>	<b>113</b>

---

### Chapter 6: LS/FS Transfer Types & Scheduling

<b>Overview.....</b>	<b>117</b>
<b>Client Initiates Transfer.....</b>	<b>118</b>
Communications Pipes .....	119

# Contents

---

Communication Initiated by I/O Request Packets .....	120
<b>Frame-Based Transfers.....</b>	<b>121</b>
<b>Transfer Types .....</b>	<b>122</b>
Isochronous Transfers .....	123
Direction of Transfers.....	123
Service Period .....	123
Bandwidth Allocation .....	123
Error Recovery .....	124
Establishing Synchronous Connections.....	125
The Problem with Isochronous Transfers .....	125
The Feedback/Feed Forwarding Solution .....	128
Synchronization Types.....	128
Source/Sink Combinations and Synchronization Methods.....	129
Asynchronous Source and Asynchronous Sink.....	130
Asynchronous Source and Synchronous Sink.....	130
Asynchronous Source and Adaptive Sink .....	130
Synchronous Source and Asynchronous Sink.....	130
Synchronous Source and Synchronous Sink .....	130
Synchronous Source and Adaptive Sink.....	130
Adaptive Source and Asynchronous Sink.....	131
Adaptive Source and Synchronous Sink.....	131
Adaptive Source and Adaptive Sink .....	131
How Endpoints Report Their Synchronization Capabilities.....	131
Feedback Data .....	131
Association Between Data Endpoint and Feedback Endpoint .....	134
Interrupt Transfers.....	134
Service Period .....	134
Bus Bandwidth Allocation.....	135
Error Recovery .....	135
Control Transfers .....	136
Bus Bandwidth Allocation.....	137
Error Recovery .....	137
Bulk Transfers.....	137
Bus Bandwidth Allocation.....	137
Error Recovery .....	139

---

## Chapter 7: Packets & Transactions

<b>Overview.....</b>	<b>141</b>
<b>Packets — The Basic Building Blocks of USB Transactions .....</b>	<b>143</b>
Synchronization Sequence .....	144
Packet Identifier .....	145
Packet-Specific Information.....	146

# Contents

---

Cyclic Redundancy Checking (CRC) .....	146
End of Packet (EOP) .....	147
<b>Token Packets</b> .....	<b>147</b>
SOF Packet .....	148
IN Packet .....	149
OUT Packet .....	150
SETUP Packet .....	151
<b>Data Packets — DATA0 and Data1</b> .....	<b>152</b>
<b>Handshake Packets</b> .....	<b>153</b>
<b>Preamble Packet</b> .....	<b>154</b>
<b>Transactions</b> .....	<b>156</b>
IN Transactions .....	156
IN Transaction Without Errors.....	157
IN Transaction with Errors.....	157
IN Transaction with No Interrupt Pending/Target Busy .....	158
IN Transaction with Target Stalled .....	159
IN Transaction During Isochronous Transfer .....	159
OUT Transactions .....	160
OUT Transaction Without Data Packet Errors.....	160
OUT Transaction with Errors.....	161
OUT Transaction — Target Unable to Accept Data .....	161
OUT Transaction With Target Stalled .....	162
OUT Transaction During Isochronous Transfer .....	162
Setup Transactions/Control Transfers .....	163
Two Stage Control Transfer .....	164
Three Stage Control Transfer with IN Data Stage .....	165
Three Stage Control Transfer with OUT Data Stage .....	166
Control Transfers With Errors .....	166

---

## Chapter 8: Error Recovery

<b>Overview</b> .....	<b>167</b>
<b>Packet Errors</b> .....	<b>168</b>
PID Checks.....	168
CRC Errors.....	169
Bit Stuff Errors.....	170
Packet-Related Error Handling.....	171
Token Packet Errors .....	171
IN Packet Errors.....	171
OUT or SETUP Packet Errors .....	171
Data Packet Errors .....	171
During OUT or SETUP Transactions.....	171
During IN Transactions .....	171

# Contents

---

Handshake Packet Errors .....	172
During OUT Transactions .....	172
During IN Transactions .....	172
Bus Time-Out.....	172
False EOPs .....	174
False EOP During Host Transmission .....	174
False EOP During Target Transmission .....	174
Data Toggle Errors .....	175
Data Toggle Procedure Without Errors .....	175
Data Toggle during OUT Transactions .....	175
Data Toggle During IN Transactions .....	178
Data Toggle Procedure with Data Packet Errors .....	179
Data Toggle and Data Packet Errors — OUT Transactions .....	180
Data Toggle and Data Packet Errors — IN Transactions .....	182
Data Toggle Procedure With Handshake Packet Errors .....	183
Data Toggle and Handshake Errors — OUT Transactions .....	184
.....	186
Data Toggle With Handshake Packet Error — IN Transaction .....	186
Special Case: Data Toggle During Control Transfer .....	188
Babbling Devices .....	189
Loss of Activity (LOA) .....	189
Babble/LOA Detection and Recovery .....	189
Frame Timer.....	189
Host to Hub Skew .....	190
Hub Repeater State Machine .....	191
Isochronous Transfers (Delivery Not Guaranteed) .....	193
Interrupt Transfer Error Recovery .....	193
Bulk Transfer Error Recovery .....	193
Control Transfer Error Recovery .....	193

---

## Chapter 9: USB Power Conservation

Power Conservation — Suspend.....	195
Device Response to Suspend .....	196
Hub Response to Suspend .....	196
Global Suspend .....	197
Initiating Global Suspend .....	197
Resume from Global Suspend .....	197
Resume Initiated by Host .....	198
Remote Wakeup from Device .....	199
Remote Wakeup via Hub Port Event .....	199
Selective Suspend .....	201
Initiating Selective Suspend .....	201

# Contents

---

Resume from Selective Suspend .....	201
Host Initiated Selective Resume .....	201
Selective Wakeup from Device .....	202
Selective Suspend When Hub is Suspended.....	204
Device Signals Resume .....	204
Port Receives Connect or Disconnect .....	206
<b>Selective Suspend Followed by Global Suspend.....</b>	<b>206</b>
<b>Resume via Reset .....</b>	<b>206</b>
Hub Frame Timer After Wakeup .....	208

---

## Part Three High Speed Device Operation

---

### Chapter 10: Overview of HS Device Operation

<b>Overview.....</b>	<b>213</b>
<b>New High-Speed Device Features.....</b>	<b>214</b>
<b>1.x USB Device Support.....</b>	<b>214</b>
<b>The 2.0 Host Controller.....</b>	<b>216</b>

---

### Chapter 11: The High-Speed Signaling Environment

<b>Overview.....</b>	<b>217</b>
<b>Detecting High-Speed Device Attachment.....</b>	<b>219</b>
Initial Device Detection.....	221
Device Reset and the Chirp Sequence.....	221
High-Speed Interfaces Idled.....	223
<b>High-Speed Differential Signaling.....</b>	<b>224</b>
Impedance Matching.....	224
High-Speed Driver Characteristics.....	226
High-Speed Idle .....	227
High-Speed Differential Receivers .....	227
High-Speed Driver/Receiver Compliance Testing.....	228
Activating Test Mode.....	229
The Test Setup .....	230
Eye Pattern Tests.....	231
Transmit Eye Pattern Tests.....	232
Receiver Eye Pattern Tests .....	233
<b>High-Speed Start of Packet &amp; Synchronization Sequence .....</b>	<b>234</b>
<b>High-Speed End of Packet (EOP) .....</b>	<b>236</b>
<b>Detection of High-Speed Device Removal .....</b>	<b>236</b>
<b>High-Speed RESET and Suspend.....</b>	<b>239</b>
Signaling RESET.....	239

# Contents

---

Signaling Suspend .....	239
Differentiating Between RESET and Suspend.....	240
<b>Chapter 12: HS Transfers, Transactions, &amp; Scheduling</b>	
<b>Overview.....</b>	<b>242</b>
<b>High-Speed Transaction Scheduling .....</b>	<b>242</b>
Microframes .....	243
Theoretical HS Bandwidth .....	243
<b>Periodic Transfers .....</b>	<b>244</b>
High-Speed Isochronous Transfers.....	244
Maximum Packet Size .....	244
Isochronous Bandwidth/Performance.....	244
Isochronous Transaction Errors.....	247
High-Speed Interrupt Transfers.....	247
Maximum Packet Size .....	247
Interrupt Bandwidth .....	247
Interrupt Transaction Errors .....	249
High-Bandwidth Transactions.....	249
Detecting High-Bandwidth Endpoints and Packet Size .....	250
Isochronous High-Bandwidth Scheduling and Protocol .....	251
High-Bandwidth Isochronous IN Transactions .....	252
High-Bandwidth Isochronous OUT Transactions .....	252
High Bandwidth Interrupt Transactions.....	253
High Bandwidth Throughput.....	254
<b>Non-Periodic Transfers .....</b>	<b>254</b>
High-Speed Bulk Transfers.....	255
Maximum Packet Size .....	255
Bulk Bandwidth .....	255
Bulk Transactions Errors .....	257
High-Speed Control Transfers .....	257
High-Speed Control Bandwidth.....	257
Ping Transactions .....	260
The Problem.....	260
The Solution.....	260
The Ping Protocol.....	261
PING Packet Handshake Responses.....	263

# **Contents**

---

## **Chapter 13: HS Error Detection and Handling**

Overview.....	265
High-Speed Bus Time-out .....	266
False EOP .....	267
HS Babbling Device Detection.....	268

---

## **Chapter 14: HS Suspend and Resume**

Overview.....	271
Entering Device Suspend .....	272
Device Resume .....	273

---

## **Part Four**

### **USB 2.0 Hub Operation with LS/FS/HS Devices**

## **Chapter 15: HS Hub Overview**

Overview.....	277
<b>USB 2.0 Hub Attached to High-Speed Port.....</b>	<b>278</b>
High-Speed Transactions.....	280
Low- and Full-Speed Transactions.....	280
<b>USB 2.0 Hub Attached to Full-Speed Port.....</b>	<b>281</b>

---

## **Chapter 16: 2.0 Hubs During HS Transactions**

Overview.....	283
<b>High-Speed Hub Repeater .....</b>	<b>284</b>
Receiver Squelch .....	285
Re-clocking the Packet.....	285
Port Selector State Machine .....	285
Elasticity Buffer .....	286
The Repeater State Machine .....	286

---

## **Chapter 17: 2.0 Hubs During LS/FS Transactions**

Overview.....	289
<b>The Structure of Split Transactions.....</b>	<b>290</b>
Isochronous Split Transaction Examples.....	291
Example Split Isochronous OUT Transaction .....	291
Example Split Isochronous IN Transaction .....	292
Example Split Transactions with Data Verification .....	293
Split OUT Sequence.....	294

# Contents

---

Split IN Sequence .....	295
<b>The Split Token Packet.....</b>	<b>296</b>
<b>The Transaction Translator .....</b>	<b>297</b>
The Major Elements of the Transaction Translator .....	297
High-Speed Handler .....	298
Periodic Transfer Start-Split Buffer .....	299
Periodic Complete-Split Buffer.....	299
Bulk/Control Buffers .....	299
Low-Speed/Full-Speed Handler .....	299
<b>Split Transaction Scheduling .....</b>	<b>300</b>
Split Transaction Scheduling Example .....	300
SOF Packets .....	300
Host Delivers Isochronous Start Split.....	301
Host Delivers Interrupt Start Split .....	302
Full- and Low-Speed Transactions Begin.....	303
Host Issues Complete-Split to Fetch Isochronous IN Data .....	304
Host Fetches Interrupt OUT Completion Status.....	305
Host Continues to Fetch Isochronous IN Data.....	306
Transaction End .....	307
High-Speed Scheduling Can Include Other Transactions .....	308
Single versus Multiple Transaction Translators .....	309
<b>Periodic Split Transactions .....</b>	<b>310</b>
Periodic Split Transaction Pipeline .....	311
High Speed Handler Receives Start Split.....	311
Start-Split Buffer.....	312
Low-Speed/Full-Speed Handler .....	312
Complete-Split Buffer.....	312
Isochronous OUT Split Transaction Sequence.....	313
Isochronous OUT Start Split .....	313
Start-Split Transaction Received with No Errors.....	315
Start-Split Transaction with Errors .....	315
Handling CRC16 During Split Isochronous OUT Transactions .....	315
Isochronous IN Split Transaction Sequence.....	316
Isochronous IN Start Split .....	316
Isochronous IN Complete Split .....	317
Complete Split Packet Error.....	317
Complete Split with MDATA.....	318
Complete Split with DATA0.....	318
Complete Split with NYET.....	318
Complete Split with ERR.....	319
Handling CRC16 During Split Isochronous IN Transactions .....	319
Interrupt Split OUT Transaction Sequence .....	319

# Contents

---

Interrupt OUT Start Split Sequence .....	319
Interrupt OUT Complete Split Sequence .....	320
Complete Split Packet Error.....	321
Complete Split with ACK.....	322
Complete Split with NYET.....	322
Complete Split with NAK .....	322
Complete Split with STALL.....	322
Complete Split with ERR.....	322
Interrupt IN Split Transaction Sequence .....	322
Interrupt IN Start Split Sequence .....	323
Interrupt IN Complete Split Sequence .....	323
Complete Split Packet Error.....	324
Complete Split with MDATA.....	324
Complete Split with DATA0/1 .....	325
Complete Split with NYET.....	325
Complete Split with NAK .....	325
Complete Split with STALL.....	326
Complete Split with ERR.....	326
Handling CRC16 During Split Interrupt IN Transactions.....	326
Non Periodic Split Transactions .....	327
Non-Periodic Split Transaction Pipeline .....	327
High Speed Handler.....	328
Non-periodic Buffers.....	328
Low-/Full-Speed Handler.....	328
Bulk/Control Split OUT Transaction Sequence .....	328
Bulk/Control OUT Start Split Sequence .....	329
Start Split with Packet Error.....	329
Start Split with ACK.....	330
Start Split with NAK .....	330
Bulk/Control OUT Complete Split Sequence .....	330
Complete Split Packet Error.....	331
Complete Split with ACK.....	331
Complete Split with NYET.....	332
Complete Split with NAK .....	332
Complete Split with STALL.....	332
Bulk/Control Split IN Transaction Sequence .....	332
Bulk/Control IN Start Split Sequence .....	332
Start Split with Packet Error.....	333
Start Split with ACK.....	334
Start Split with NAK .....	334
Bulk/Control IN Complete Split Sequence .....	334
Complete Split Packet Error.....	335

# Contents

---

Complete Split with NYET.....	336
Complete Split with NAK .....	336
Complete Split with STALL.....	336

---

## Part Five USB Device Configuration

---

### Chapter 18: Configuration Process

Overview.....	339
<b>The Configuration Software Elements .....</b>	<b>341</b>
USB Host Controller Driver .....	342
Configuration Software.....	342
Default Control Pipe.....	342
Resource Management.....	343
Device Client Software.....	343
<b>Root Hub Configuration.....</b>	<b>343</b>
Each Device Is Isolated for Configuration.....	344
Reset Forces Device to Default Address (zero).....	345
Host Assigns a Unique Device Address.....	345
Host Software Verifies Configuration.....	345
Power Requirements .....	345
Bus Bandwidth.....	346
Configuration Value Is Assigned .....	346
Client Software Is Notified.....	346

---

### Chapter 19: USB Device Configuration

Overview.....	347
<b>Summary of Configuration Process.....</b>	<b>348</b>
<b>How Software Detects Device Attachment &amp; Speed .....</b>	<b>348</b>
Polling the Status Change Endpoint .....	349
Getting Port Status .....	350
<b>Resetting the Port.....</b>	<b>352</b>
<b>Reading and Interpreting the USB Descriptors .....</b>	<b>353</b>
The Standard Descriptors .....	353
How Software Accesses the Descriptors .....	354
Device Descriptor.....	355
Class Code Field.....	358
Maximum Packet Size Zero.....	359
Manufacturer, Product, Serial Number .....	359
Number of Configurations .....	359
Device Qualifier Descriptor.....	360

# Contents

---

Configuration Descriptors.....	361
Number of Interfaces.....	361
Configuration Value.....	361
Attributes and Maximum Power.....	361
Other Speed Configuration Descriptor.....	363
Interface Descriptors.....	364
Interface Number and Alternate Setting .....	364
Number of Endpoints .....	365
Interface Class and Subclass.....	366
Protocol .....	366
Endpoint Descriptors .....	367
Device States .....	371
Attached State.....	371
Powered State .....	372
Default State.....	372
Addressed State.....	372
Configured State .....	372
Suspend State.....	373
Client Software Configuration.....	374

---

## Chapter 20: Hub Configuration

Configuring the Hub .....	376
The Default Pipe.....	376
The Status Change Pipe .....	376
Reading the Hub's Descriptors .....	377
1.x Hub Descriptors .....	378
Hub's Standard Device Descriptor.....	379
Hub Configuration Descriptor.....	380
Number of Interfaces.....	381
Configuration Value.....	381
Bus- or Self-Powered Hub .....	381
Maximum Bus Power Consumed .....	381
Hub Interface Descriptor .....	383
Status Endpoint Descriptor .....	384
Status Change Endpoint Address/Transfer Direction.....	385
Transfer Type .....	385
Maximum Data Packet Size.....	385
Polling Interval.....	385
Hub Class Descriptor .....	387
Power Switching Mode Implemented .....	387
Compound Device or Hub Only .....	390
Over-Current Protection Mode.....	390

# Contents

---

Power On to Power Good Delay .....	390
Maximum Bus Current for Hub Controller.....	390
Device Removable/Non-removable.....	390
Port Power Mask.....	391
<b>High-Speed Capable Hub Descriptors .....</b>	<b>391</b>
Descriptors When Hub Is Operating at Full Speed .....	391
The 2.0 Hub's Class-Specific Descriptor .....	394
<b>Powering the Hub .....</b>	<b>397</b>
<b>Checking Hub Status.....</b>	<b>397</b>
Detecting Hub Status Changes .....	397
Reading the Hub Status Field.....	398
Reading Port Status .....	399
Enabling the Device.....	399
<b>Summary of Hub Port States .....</b>	<b>399</b>

---

## Chapter 21: Device Classes

<b>Overview.....</b>	<b>403</b>
<b>Device Classes .....</b>	<b>406</b>
<b>Audio Device Class.....</b>	<b>407</b>
Standard Audio Interface Requirements.....	408
Synchronization Types.....	409
Audio Class-Specific Descriptors .....	409
Audio Class-Specific Requests .....	410
<b>Communications Device Class .....</b>	<b>410</b>
Communications Device Interfaces.....	411
Communications Class-Specific Descriptors .....	412
Communications Class-Specific Requests.....	412
<b>Display Device Class.....</b>	<b>412</b>
The Standard Display Device Class Interface.....	413
Display Device-Specific Descriptors .....	413
Device-Specific Requests.....	414
<b>Mass Storage Device Class .....</b>	<b>414</b>
Standard Mass Storage Interface .....	415
Control Endpoint .....	415
Bulk Transfer Endpoints .....	416
Interrupt Endpoint.....	416
General Mass Storage Subclass.....	416
CD-ROM Subclass.....	416
Tape Subclass.....	417
Solid State Subclass.....	417
Class- and Device-Specific USB Requests .....	418

# **Contents**

---

---

## **Part Six**

### **USB Software Overview**

---

#### **Chapter 22: Overview of USB Host Software**

<b>USB Software .....</b>	<b>421</b>
Function Layer.....	422
Device Layer .....	422
Interface Layer.....	423
The Software Components .....	424
<b>USB Driver (USBD) .....</b>	<b>426</b>
<b>Configuration Management.....</b>	<b>426</b>
USB Elements Requiring Configuration .....	426
Allocating USB Resources.....	427
Verifying Power .....	427
Tracking and Allocating Bus Bandwidth.....	428
Bus Bandwidth Reclamation.....	429
<b>Data Transfer Management .....</b>	<b>429</b>
<b>Providing Client Services (The USB Driver Interface).....</b>	<b>430</b>
Pipe Mechanisms .....	430
Client Pipe Requirements .....	430
Command Mechanisms .....	431

---

## **Appendix**

---

#### **Appendix A: Standard Device Requests**

<b>Overview.....</b>	<b>435</b>
<b>Standard Device Requests.....</b>	<b>436</b>
<b>Set/Clear Feature .....</b>	<b>439</b>
Device Remote Wakeup .....	439
Endpoint Stall .....	439
<b>Set/Get Configuration .....</b>	<b>440</b>
<b>Set/Get Descriptor.....</b>	<b>440</b>
<b>Set/Get Interface .....</b>	<b>441</b>
<b>Get Status.....</b>	<b>442</b>
Device Status.....	442
Self-Powered Bit.....	442
Remote Wakeup Bit.....	443
Port Test Bit.....	443
Endpoint Status .....	443

# Contents

---

<b>Sync Frame .....</b>	<b>444</b>
<b>Device Tests .....</b>	<b>444</b>
High-speed Driver/Receiver Compliance Testing .....	444
Activating Test Mode.....	444

---

## Appendix B: Hub Requests

<b>Overview.....</b>	<b>447</b>
<b>Hub Request Types .....</b>	<b>448</b>
Standard Requests and Hub Response.....	449
<b>Hub Class Requests .....</b>	<b>450</b>
<b>Get/Set Descriptor Request.....</b>	<b>452</b>
<b>Get Hub Status Request.....</b>	<b>452</b>
Hub Status Fields.....	453
Local Power Status .....	453
Over-Current Indicator .....	453
Hub State Change Fields.....	454
Local Power Status Change.....	454
Over-Current Indicator Change .....	454
<b>Set/Clear Hub Feature Request .....</b>	<b>455</b>
Hub Local Power Change Request.....	456
Hub Over-Current Change Request.....	456
<b>Get Port Status Request .....</b>	<b>456</b>
Port Status Fields.....	457
Current Connect Status Field.....	457
Port Enabled/Disabled .....	457
Suspend .....	458
Over-Current Indicator .....	458
Reset.....	458
Port Power .....	458
Low-Speed Device Attached .....	459
High-Speed Device Attached.....	459
Port Test .....	459
Port Indicator Control.....	459
Port Change Fields.....	459
Current Status Change .....	460
Port Enable/Disable Change .....	460
Suspend Change (Resume Complete) .....	460
Over-Current Indicator Change .....	461
Reset Complete.....	461
<b>Set/Clear Port Feature .....</b>	<b>461</b>
<b>Port Test Modes.....</b>	<b>462</b>
<b>Get Bus State .....</b>	<b>463</b>

# **Contents**

---

## **Appendix C: Universal Host Controller**

<b>Overview</b> .....	<b>465</b>
<b>Universal Host Controller Transaction Scheduling</b> .....	<b>465</b>
Universal Host Controller Frame List Access.....	466
UHC Transfer Scheduling Mechanism .....	467
Bus Bandwidth Reclamation .....	468
<b>Transfer Descriptors</b> .....	<b>468</b>
<b>Queue Heads</b> .....	<b>473</b>
<b>UHC Control Registers</b> .....	<b>474</b>

## **Appendix D: Open Host Controller**

<b>Overview</b> .....	<b>477</b>
<b>Open Host Controller Transfer Scheduling</b> .....	<b>477</b>
The Open Host Controller Transfer Mechanism.....	478
The ED and TD List Structure .....	480
Interrupt and Isochronous Transfer Processing.....	480
Control and Bulk Transfer Processing.....	480
The Done Queue .....	481
Interrupt Transfer Scheduling.....	481
<b>Endpoint Descriptors</b> .....	<b>483</b>
Transfer Descriptors .....	485
General Transfer Descriptor .....	486
Isochronous Transfer Descriptor .....	488
<b>The Open Host Controller Registers</b> .....	<b>492</b>

# Figures

---

1-1	System Resources Used by Legacy Peripheral Devices .....	14
1-2	Connectors at Backplane.....	17
1-3	USB Device Connections.....	22
2-1	USB System Implemented in a PCI-Based Platform.....	26
2-2	USB Controller Integrated into I/O Hub Chip.....	27
2-3	1.x Systems Support Only Low- and Full-Speed Devices.....	28
2-4	Full-Speed Transactions Do Not Reach Low-Speed Devices .....	29
2-5	Conceptual View of Transaction Generation — Example 1 .....	31
2-6	Conceptual View of Transaction Generation — Example 2 .....	32
2-7	Conceptual View of 1ms Frame Generation.....	33
2-8	Example of USB Devices That Share Bus Bandwidth.....	35
2-9	USB 2.0 System with Low-, Full-, and High-Speed Devices Attached .....	37
2-10	Low- and Full-Speed Devices Attached to Ports of the Root, 1.x, and 2.0 Hubs.....	38
2-11	Split IN Transaction Sequence .....	39
2-12	Example 2.0 Controller with Three 1.x Host Controllers Used for Low- and Full-Speed Support.....	40
2-13	Example of High-Speed Devices Attached to 2.0 Root Hub and High-Speed Hub.....	41
2-14	Conceptual View of Host Controller Generation of Microframes.....	42
2-15	Bandwidth Comparison Between 12MHz Frames and 480MHz Microframes.....	43
2-16	Communication Flow in a USB System.....	45
2-17	Block Diagram of Major Root Hub Functions .....	49
2-18	USB Hub Types .....	50
2-19	Primary Hub Functions.....	51
2-20	Hub Repeater Performing Downstream and Upstream Connectivity .....	52
2-21	The Communications Model.....	56
2-22	USB Devices Performing Transfers During Frame .....	58
2-23	Relationship Between IRPs, Transfers, Frames, and Packets.....	59
2-24	Standard Descriptors.....	61
2-25	Standard Descriptors with Two Configurations .....	62
2-26	Device Framework — Software’s View of Hardware .....	64
2-27	USB’s Tiered Star Topology .....	68
3-1	A View of the Series A Plug .....	70
3-2	Cross Section of a Low-Speed Cable Segment.....	72
3-3	Cross Section of a High-Speed Cable Segment.....	73
4-1	Minimum Cable Voltage and Voltage Drop Budget .....	78
4-2	Bus-Powered Hub with Embedded Function and Four Ports .....	82
4-3	Low-Power USB Function .....	83
4-4	Bus-Powered Function (High Power) .....	85
4-5	Self-Powered Hub with Embedded Function.....	88
4-6	Self-Powered Device.....	90
5-1	Signaling Interface USB Hub and Attached USB Full-Speed Device.....	95
5-2	Hub Port with No Device Connected .....	96
5-3	Connect Sequence from Port Power through Device Reset.....	97
5-4	Full-Speed Device Detection .....	98
5-5	Signal States During FS Device Attachment.....	99
5-6	Low-Speed Device Detection .....	100

# **Figures**

---

5-7	Line States During Low-Speed Device Connection.....	101
5-8	Signaling State During Device Disconnect.....	102
5-9	Bus Idle Line States.....	103
5-10	Reset Signaling States.....	104
5-11	Signaling Interface Between Hub and Device.....	105
5-12	Full-Speed Differential Drivers and Receivers .....	106
5-13	CMOS Buffer with Series Resistors Achieve Specified Output Impedance.....	107
5-14	Full-Speed Driver and Receiver Waveforms .....	108
5-15	Start of Packet Is Recognized at the Beginning of the Synchronization Sequence.....	109
5-16	Full- or Low-Speed EOP signaling.....	110
5-17	Transfers Across USB Cables Employ NRZI Encoding and Differential Signaling.....	111
5-18	NRZI Encoded Data .....	112
5-19	Stuffed Bit.....	113
5-20	USB Signaling Levels.....	115
6-1	Communications Pipes Between Client Software's Memory Buffer and Device Endpoints .....	120
6-2	Client Request Converted to USB Transactions.....	121
6-3	Isochronous Application Using USB CD-ROM and Speakers.....	126
6-4	Example of Source Device Delivering Isochronous Data to the Bus.....	127
6-5	Example of Sink Device Receiving Isochronous Data from the Bus.....	127
6-6	Format of Feedback Data for Full-Speed Devices.....	133
6-7	Format of Feedback Data for High-Speed Device.....	133
7-1	The Layers Involved in USB Transfers .....	142
7-2	Many USB Transactions Consist of Three Phases.....	143
7-3	Packet Format .....	144
7-4	Synchronization Sequence.....	144
7-5	Packet Identifier Format .....	146
7-6	End of Packet signaling.....	147
7-7	Format of an SOF Packet.....	149
7-8	IN Token Packet Format .....	150
7-9	OUT Token Packet Format .....	151
7-10	SETUP Token Packet Format .....	151
7-11	DATA0 Packet Format .....	152
7-12	DATA1 Packet Format .....	153
7-13	Handshake Packet Formats .....	154
7-14	Preamble Packet Format .....	156
7-15	IN Transaction Without Errors .....	157
7-16	IN Transaction With Data Phase Errors .....	158
7-17	IN Transaction With Target Temporarily Unable to Return Data.....	158
7-18	IN Transaction with Target Stalled .....	159
7-19	IN Transaction During Isochronous Transfer.....	160
7-20	OUT Transaction Without Errors .....	161
7-21	OUT Transaction with Data Packet Errors.....	161
7-22	OUT Transaction to Target That is Unable to Accept Data.....	162
7-23	OUT Transaction to Stalled Endpoint.....	162
7-24	OUT Transaction During Isochronous Transfer.....	163

# Figures

---

7-25	Format of a Two Stage Control Transfer .....	165
7-26	Control Transfer Requesting Data from Target.....	165
7-27	Control Transfer Issuing a Command to a Target's Control Endpoint .....	166
8-1	PID Check .....	169
8-2	Total Trip Delay .....	173
8-3	OUT Transaction With Data Toggle Sequence and No Errors.....	177
8-4	IN Transaction With Data Toggle Sequence and No Errors.....	179
8-5	OUT Transaction With Data Toggle and Data Packet Errors .....	180
8-6	IN Transaction With Data Toggle and Data Packet Errors.....	182
8-7	OUT Transaction With Data Toggle and Handshake Errors .....	184
8-8	IN Transaction With Data Toggle and Handshake Errors .....	186
8-9	Data Toggle During Control Transfers.....	188
8-10	Hub EOF Points.....	190
8-11	EOF Timing Ranges.....	191
8-12	Hub Repeater State Diagram.....	192
9-1	Host Initiated Resume .....	198
9-2	Global Resume Signaling Due to Wakeup from Target Device.....	200
9-3	Selective Resume Signaled by Target Device .....	203
9-4	Device Initiated Selective Resume to Suspended Hub.....	205
9-5	Resume with Selective and Global Suspend.....	207
9-6	Repeater State Machine With Suspend and Resume Transitions.....	209
10-1	USB 2.0 Example Topology .....	215
11-1	High-Speed Capable Ports Must Support a Variety of Speeds.....	218
11-2	High-Speed signaling Interface .....	220
11-3	Sequence of Events from Device Connect to High-Speed Operation .....	221
11-4	Chirp Sequence Used to Detect High-Speed Capable Device .....	223
11-5	High-Speed Cable Termination .....	225
11-6	Interface Elements Used During High-Speed Differential Signaling.....	226
11-7	SOP Detection.....	228
11-8	Test Points .....	231
11-9	Test Packet Contents.....	232
11-10	Example Eye Diagram for Transmit Test .....	233
11-11	Example Eye Diagram for Receiver Sensitivity Test .....	234
11-12	High-Speed Synchronization Sequence and SOP .....	235
11-13	Squelch Detection Can Cause Hubs to Drop up to Four Bits from Synchronization Sequence .....	235
11-14	High-Speed EOP Detection .....	236
11-15	Device Removal is Checked at End of MicroSOF Packet.....	237
11-16	Disconnect Envelope Detector .....	238
12-1	Bandwidth Difference Between Full-Speed Frame and High-Speed Microframe .....	243
12-2	Isochronous Packet Overhead .....	245
12-3	Interrupt Transaction Overhead.....	248
12-4	Minimum and Maximum Packet Sizes for High-Bandwidth Transactions .....	251
12-5	Data Packet Sequence Used During High-Bandwidth Isochronous IN Transactions .....	252

# Figures

---

12-6	Data Packet Sequence Used During High-Bandwidth Isochronous OUT Transactions.....	253
12-7	Bulk Transaction Overhead.....	255
12-8	Control Transfer Overhead - Setup Stage .....	258
12-9	Control Transfer Overhead - Data Stage.....	258
12-10	Control Transfer Overhead - Status Stage.....	259
12-11	PING Transaction versus OUT Transaction .....	261
12-12	Host Ping Processing Overview .....	262
12-13	Endpoint Ping Processing.....	262
13-1	Worst-Case Round Trip Delay Between Host and Function.....	267
13-2	Babbling Device Detection Model.....	269
13-3	Separation of EOF Sample Points.....	270
14-1	Device Detection and Entry into Suspend State.....	273
15-1	Example USB 2.0 Topology with Old and New Hubs.....	278
15-2	Packet Routing Options for High-Speed Hub.....	279
15-3	Split Transaction are Required to Access Low- or Full-Speed DevicesThat Attach to High-Speed Hubs .....	281
15-4	Example Topology Where Devices Do Not Operate Optimally.....	282
16-1	Repeater Function Within Hub.....	284
16-2	Repeater State Machine.....	287
17-1	Packet Flow Through Hub with LS/FS and HS Devices Attached.....	290
17-2	Example Isochronous OUT Split Transaction.....	292
17-3	Example Isochronous IN Split Transaction.....	293
17-4	Example OUT Split Transaction With Data Delivery Verification.....	294
17-5	Example IN Split Transaction With Data Delivery Verification.....	295
17-6	Split Token Packet Definition.....	297
17-7	Major Elements Within Transaction Translator .....	298
17-8	Example Split Transaction Sequence — Step 1.....	301
17-9	Example Split Transaction Sequence — Step 2.....	302
17-10	Example Split Transaction Sequence — Step 3.....	303
17-11	Example Split Transaction Sequence — Step 4.....	304
17-12	Example Split Transaction Sequence — Step 5.....	305
17-13	Example Split Transaction Sequence — Step 6.....	306
17-14	Example Split Transaction Sequence — Step 7.....	307
17-15	Example Split Transaction Sequence — Step 8.....	308
17-16	Example Split Transaction Sequence — Step 9.....	309
17-17	Single or Multiple Transaction Translators.....	310
17-18	Periodic Split Transaction Pipeline .....	311
17-19	Isochronous Start Split Packet Sequence .....	313
17-20	Start-Split Encoding for Isochronous OUT Transactions.....	314
17-21	Sequence of Packets in Start-Split Transaction During Isochronous IN.....	316
17-22	Sequence of Complete-Split Transaction During Isochronous IN.....	318
17-23	Interrupt OUT Start-Split Packet Sequence.....	320
17-24	Interrupt OUT Complete-Split Packet Sequence.....	321
17-25	Interrupt IN Start Split Sequence.....	323
17-26	Complete Split Transaction Sequence During an Interrupt IN transaction.....	324

# Figures

---

17-27	Non-Periodic Split Transaction Pipeline .....	327
17-28	Bulk/Control OUT Start-Split Sequence .....	329
17-29	Bulk/Control OUT Complete-Split Sequence .....	331
17-30	Bulk/Control IN Start-Split Sequence .....	333
17-31	Bulk/Control IN Complete Split Sequence.....	335
18-1	The Software Elements Used During Configuration.....	341
18-2	Root Hub's Control and Status Change Endpoints .....	344
19-1	Hub and Port Status Change Bitmap.....	350
19-2	Descriptor Tree Containing Alternate Interface Settings.....	365
20-1	Required Hub Endpoints.....	377
20-2	Standard Hub Descriptors.....	378
20-3	Hub and Port Status Change Bitmap .....	398
21-1	CD-ROM Supporting Mass Storage and Audio Interfaces.....	405
22-1	Device Framework — Software's View of Hardware .....	423
22-2	Software Layers.....	425
A-1	Format of Setup Transaction that Specifies the Device Request Being Performed.....	436
B-1	Format of Setup Transaction That Specifies the Device Request Being Performed.....	447
C-1	Universal Host Controller Transfer Scheduling.....	466
C-2	Frame List Access.....	467
C-3	Transfer Mechanism and Execution Order .....	469
C-4	Transfer Descriptor Format .....	470
C-5	The Queue Head Link and Element Link Pointers.....	473
D-1	USB Transfer Scheduling .....	478
D-2	The Transfer Scheduling Mechanism .....	479
D-3	Transfer Queues .....	481
D-4	Interrupt Scheduling .....	482
D-5	Endpoint Descriptor Format .....	483
D-6	Transfer Descriptor Format .....	486
D-7	Isochronous Transfer Descriptor .....	490
D-8	Open Host Controller Registers.....	493