Introduction

(This introduction is not a part of IEEE Std 1364-1995, IEEE Standard Hardware Description Language Based on the Verilog® Hardware Description Language.)

The Verilog® Hardware Description Language (Verilog HDL) was designed to be simple, intuitive, and effective at multiple levels of abstraction in a standard textual format for a variety of design tools, including verification simulation, timing analysis, test analysis, and synthesis. The Verilog HDL was designed by Phil Moorby during the winter of 1983–1984, and it was introduced into the EDA market in 1985 as the cornerstone of a verification simulator product.

The Verilog HDL contains a rich set of built-in primitives, including logic gates, user-definable primitives, switches, and wired logic. It also has device pin-to-pin delays and timing checks. The mixing of abstract levels is essentially provided by the semantics of two data types: nets and registers. Continuous assignments, in which expressions of both registers and nets can continuously drive values onto nets, provide the basic structural construct. Procedural assignments, in which the results of calculations involving register and net values can be stored into registers, provide the basic behavioral construct. A design consists of a set of modules, each of which has an I/O interface and a description of its function, which can be structural, behavioral, or a mix. These modules are formed into a hierarchy and are interconnected with nets.

The Verilog language is extensible via the Programming Language Interface (PLI). The PLI is a collection of routines that allows foreign functions to access information contained in a Verilog HDL description of the design and facilitates dynamic interaction with simulation. Applications of PLI include connecting to a Verilog HDL simulator with other simulation and CAD systems, customized debugging tasks, delay calculators, and annotators.

The language that influenced Verilog HDL the most was HILO-2, which was developed at Brunel University in England under a contract to produce a test generation system for the British Ministry of Defense. HILO-2 successfully combined the gate and register transfer levels of abstraction and supported verification simulation, timing analysis, fault simulation, and test generation.

In 1990, Cadence Design Systems placed the Verilog HDL into the public domain and the independent Open Verilog International (OVI) was formed to manage and promote Verilog HDL.

In 1992, the Board of Directors of OVI began an effort to establish Verilog HDL as an IEEE standard. With many designers all over the world designing electronic circuits with Verilog HDL, this idea was enthusiastically received by the Verilog user community. When the Project Authorization Request (1364) was approved by the IEEE in 1993, a working group was formed and the first meeting was held on October 14, 1993.