

Contents

Foreword	xvii
Preface	xix
Acknowledgments	xxi
Chapter 1: Data Converter History	3
Section 1-1: Early History	5
The Early Years: Telegraph to Telephone	6
The Invention of PCM	8
The Mathematical Foundations of PCM	9
The PCM Patents of Alec Harley Reeves	10
PCM and the Bell System: World War II through 1948	11
Op Amps and Regenerative Repeaters: Vacuum Tubes to Solid-State	13
Section 1-2: Data Converters of the 1950s and 1960s.....	19
Commercial Data Converters: 1950s.....	19
Commercial Data Converter History: 1960s	20
Data Converter Architectures	23
Section 1-3: Data Converters of the 1970s	27
Monolithic Data Converters of the 1970s.....	28
Bipolar Process IC DACs of the 1970s	28
CMOS IC DACs of the 1970s	29
Monolithic ADCs of the 1970s.....	31
Hybrid Data Converters of the 1970s	32
Modular Data Converters of the 1970s.....	35
Section 1-4: Data Converters of the 1980s	39
Monolithic DACs of the 1980s.....	40
Monolithic ADCs of the 1980s.....	41
Monolithic Flash ADCs of the 1980s	42
Hybrid and Modular DACs and ADCs of the 1980s	42
Section 1-5: Data Converters of the 1990s	45
Monolithic DACs of the 1990s	46
Monolithic ADCs of the 1990s.....	48
Hybrid and Modular DACs and ADCs of the 1990s	52
Section 1-6: Data Converters of the 2000s	53
Chapter 2: Fundamentals of Sampled Data Systems	57
Section 2-1: Coding and Quantizing	57
Unipolar Codes	59
Gray Code.....	61
Bipolar Codes	62

Contents

Complementary Codes	65
DAC and ADC Static Transfer Functions and DC Errors	66
Section 2-2: Sampling Theory	73
The Need for a Sample-and-Hold Amplifier (SHA) Function	74
The Nyquist Criteria	76
Baseband Antialiasing Filters	78
Undersampling (Harmonic Sampling, Bandpass Sampling, IF Sampling, Direct IF-to-Digital Conversion)	80
Antialiasing Filters in Undersampling Applications	81
Section 2-3: Data Converter AC Errors	83
Theoretical Quantization Noise of an Ideal N-Bit Converter	83
Noise in Practical ADCs	88
Equivalent Input Referred Noise	89
Noise-Free (Flicker-Free) Code Resolution	89
Dynamic Performance of Data Converters	90
Integral and Differential Nonlinearity Distortion Effects	90
Harmonic Distortion, Worst Harmonic, Total Harmonic Distortion (THD), Total Harmonic Distortion Plus Noise (THD + N)	91
Signal-to-Noise-and-Distortion Ratio (SINAD), Signal-to-Noise Ratio (SNR), and Effective Number of Bits (ENOB)	91
Analog Bandwidth	92
Spurious Free Dynamic Range (SFDR)	93
Two-Tone Intermodulation Distortion (IMD)	94
Second- and Third-Order Intercept Points, 1 dB Compression Point	95
Multitone Spurious Free Dynamic Range	96
Wideband CDMA (WCDMA) Adjacent Channel Power Ratio (ACPR) and Adjacent Channel Leakage Ratio (ADLR)	97
Noise Power Ratio (NPR)	98
Noise Factor (F) and Noise Figure (NF)	100
Aperture Time, Aperture Delay Time, and Aperture Jitter	106
A Simple Equation for the Total SNR of an ADC	108
ADC Transient Response and Overvoltage Recovery	109
ADC Sparkle Codes, Metastable States, and Bit Error Rate (BER)	111
DAC Dynamic Performance	115
DAC Settling Time	115
Glitch Impulse Area	116
DAC SFDR and SNR	117
Measuring DAC SNR with an Analog Spectrum Analyzer	118
DAC Output Spectrum and $\sin(x)/x$ Frequency Roll-off	119
Oversampling Interpolating DACs	120
Section 2-4: General Data Converter Specifications.....	123
Overall Considerations	123
Logic Interface Issues	124
Data Converter Logic: Timing and other Issues	125
Section 2-5: Defining the Specifications.....	127

Chapter 3: Data Converter Architectures	147
Section 3-1: DAC Architectures	147
DAC Output Considerations	148
Basic DAC Structures	149
The Kelvin Divider (String DAC)	149
Thermometer (Fully-Decoded) DACs	151
Binary-Weighted DACs	153
R-2R DACs	155
Segmented DACs	159
Oversampling Interpolating DACs	163
Multiplying DACs	164
Intentionally Nonlinear DACs	164
Counting, Pulsewidth-Modulated (PWM) DACs	167
Cyclic Serial DACs	167
Other Low Distortion Architectures	169
DAC Logic Considerations	170
Section 3-2: ADC Architectures	175
The Comparator: A 1-Bit ADC	178
High Speed ADC Architectures	180
Flash Converters	180
Successive Approximation ADCs	185
Subranging, Error Corrected, and Pipelined ADCs	190
Serial Bit-Per-Stage Binary and Gray Coded (Folding) ADCs	203
Counting and Integrating ADC Architectures	211
A. H. Reeves' 5-Bit Counting ADC	211
Charge Run-Down ADC	212
Ramp Run-Up ADC	212
Tracking ADC	213
Voltage-to-Frequency Converters (VFCs)	214
Dual Slope/Multislope ADCs	218
Optical Converters	220
Resolver-to-Digital Converters (RDCs) and Synchros	221
Section 3-3: Sigma-Delta Converters	231
Historical Perspective	231
Sigma-Delta ($\Sigma-\Delta$) or Delta-Sigma ($\Delta-\Sigma$)?	234
Basics of Sigma-Delta ADCs	235
Idle Tone Considerations	240
Higher Order Loop Considerations	241
Multibit Sigma-Delta Converters	242
Digital Filter Implications	243
Multistage Noise Shaping (MASH) Sigma-Delta Converters	244
High Resolution Measurement Sigma-Delta ADCs	245
Sigma-Delta DACs	249
Chapter 4: Data Converter Process Technology	257
Section 4-1: Early Processes	257
Vacuum Tube Data Converters	257

Contents

Solid State, Modular, and Hybrid Data Converters	259
Calibration Processes.....	262
Section 4-2: Modern Processes.....	265
Bipolar Processes.....	265
Thin Film Resistor Processes	265
Complementary Bipolar (CB) Processes.....	266
CMOS Processes	266
Data Converter Processes and Architectures	268
Section 4-3: Smart Partitioning	273
When Complete Integration Isn't the Optimal Solution.....	273
Why Smart Partitioning is Necessary	276
What's Changing?	277
Chapter 5: Testing Data Converters	283
Section 5-1: Testing DACs	283
Static DAC Testing	283
End-Point Errors.....	284
Linearity Errors	286
Superposition and DAC Errors.....	286
Measuring DAC DNL and INL Using Superposition	287
Measuring DAC INL and DNL Where Superposition Does Not Hold	290
Testing DACs for Dynamic Performance	292
Settling Time	292
Glitch Impulse Area	293
Oscilloscope Measurement of Settling Time and Glitch Impulse Area	294
Distortion Measurements	295
Section 5-2: Testing ADCs	303
A Brief Historical Overview of Data Converter Specifications and Testing	303
Static ADC Testing	304
Back-to-Back Static ADC Testing.....	306
Crossplot Measurements of ADC Linearity	309
Servo-Loop Code Transition Test.....	310
Computer-Based Servo-Loop ADC Tester	311
Histogram (Code Density) Test with Linear Ramp Input	312
Dynamic ADC Testing.....	317
Manual “Back-to-Back” Dynamic ADC Testing	317
Measuring Effective Number of Bits (ENOB) Using Sinewave Curve Fitting.....	320
FFT Basics.....	322
FFT Test Setup Configuration and Measurements	329
Verifying the FFT Accuracy	335
Generating Low Distortion Sinewave Inputs	335
Noise Power Ratio (NPR) Testing.....	337
Measuring ADC Aperture Jitter Using the Locked-Histogram Test Method	338
Measuring Aperture Delay Time	340
Measuring ADC Aperture Jitter Using FFTs.....	340
Measuring ADC Analog Bandwidth Using FFTs	342
Settling Time	343

Overvoltage Recovery Time	344
Video Testing, Differential Gain and Differential Phase	344
Bit Error Rate (BER) Tests	348
Chapter 6: Interfacing to Data Converters.....	359
Section 6-1: Driving ADC Analog Inputs.....	359
Amplifier DC and AC Performance Considerations	361
Rail-Rail Input Stages.....	362
Output Stages.....	365
Gain and Level-Shifting Circuits Using Op Amps	367
Op Amp AC Specifications and Data Converter Requirements	369
Driving High Resolution Σ-Δ Measurement ADCs.....	371
Driving Single-Ended Input Single-Supply 1.6 V to 3.6 V Successive Approximation ADCs....	372
Driving Single-Supply ADCs with Scaled Inputs	373
Driving Differential Input CMOS Switched Capacitor ADCs	374
Single-Ended Drive Circuits for Differential Input CMOS ADCs	376
Differential Input ADC Drivers	378
Driving ADCs with Differential Amplifiers	382
Dual Op Amp Drivers.....	383
Fully Integrated Differential Amplifier Drivers.....	384
Driving Differential Input ADCs with Integrated Differential Drivers	387
Section 6-2: ADC and DAC Digital Interfaces(and Related Issues)	397
Power-On Initialization of Data Converters	397
Initialization of Data Converter Internal Control Registers.....	398
Low Power, Sleep, and Standby Modes	398
Single-Shot Mode, Burst Mode, and Minimum Sampling Frequency	399
ADC Digital Output Interfaces.....	400
ADC Serial Output Interfaces	400
ADC Serial Interface to DSPs	403
ADC Parallel Output Interfaces.....	405
DAC Digital Input Interfaces.....	408
DAC Serial Input Interfaces to DSPs	410
DAC Parallel Input Interfaces to DSPs.....	411
Section 6-3: Buffering DAC Analog Outputs	415
Differential to Single-Ended Conversion Techniques	416
Single-Ended Current-to-Voltage Conversion	418
Differential Current-to-Differential Voltage Conversion	420
An Active Low-Pass Filter for Audio DAC	420
Section 6-4: Data Converter Voltage References	423
Section 6-5: Sampling Clock Generation	427
Oscillator Phase Noise and Jitter	430
“Hybrid” Clock Generators	437
Driving Differential Sampling Clock Inputs	438
Sampling Clock Summary.....	439
Chapter 7: Data Converter Support Circuits.....	443
Section 7-1: Voltage References	443
Precision Voltage References	443

Contents

Types of Voltage References.....	444
Bandgap References	446
Buried Zener References	451
XFET References	452
Voltage Reference Specifications	455
Tolerance	455
Drift	455
Supply Range	456
Load Sensitivity.....	456
Line Sensitivity.....	457
Noise.....	457
Scaled References.....	459
Voltage Reference Pulse Current Response.....	460
Low Noise References for High Resolution Converters	462
Section 7-2: Low Dropout Linear Regulators	465
Linear Voltage Regulator Basics.....	465
Pass Devices and their Associated Trade Offs.....	468
Low Dropout Regulator Architectures	472
The anyCAP Low Dropout Regulator Family.....	475
Design Features Related to DC Performance.....	475
Design Features Related to AC Performance	476
A Basic Pole-Splitting Topology.....	477
The anyCAP Pole-Splitting Topology	477
The anyCAP LDO series devices	478
Functional Diagram and Basic 50 mA LDO Regulator	479
LDO Regulator Thermal Considerations	481
LDO Regulator Controllers	485
Regulator Controller Differences	485
A Basic 5 V/1 A LDO Regulator Controller	486
Selecting the Pass Device	487
Thermal Design	488
Sensing Resistors for LDO Controllers.....	489
PCB Layout Issues	490
A 2.8 V/8 A LDO Regulator Controller	491
Section 7-3: Analog Switches and Multiplexers	493
CMOS Switch Basics	494
Error Sources in the CMOS Switch.....	496
Applying the Analog Switch	504
1 GHz CMOS Switches.....	508
Video Switches and Multiplexers	508
Video Crosspoint Switches.....	511
Digital Crosspoint Switches	512
Switch and Multiplexer Families from Analog Devices.....	512
Parasitic Latchup in CMOS Switches and Muxes.....	512
Section 7-4: Sample-and-Hold Circuits.....	519
Introduction and Historical Perspective	519

Basic SHA Operation	521
Track Mode Specifications	522
Track-to-Hold Mode Specifications	522
Hold Mode Specifications	526
Hold-to-Track Transition Specifications	528
SHA Architectures.....	529
Internal SHA Circuits for IC ADCs.....	531
SHA Applications.....	533
Chapter 8: Data Converter Applications	539
Section 8-1: Precision Measurement and Sensor Conditioning.....	539
Applications of Precision Measurement Σ-Δ ADCs.....	540
Weigh Scale Design Analysis Using the AD7730 ADC.....	544
Thermocouple Conditioning Using the AD7793.....	549
Direct Digital Temperature Measurements.....	551
Microprocessor Substrate Temperature Sensors.....	555
Applications of ADCs in Power Meters	558
Section 8-2: Multichannel Data Acquisition Systems.....	563
Data Acquisition System Configurations.....	563
Multiplexing	564
Filtering Considerations in Data Acquisition Systems	567
Complete Data Acquisition Systems on a Chip.....	568
Multiplexing Inputs to Σ-Δ ADCs	570
Simultaneous Sampling Systems.....	572
Data Distribution Systems	574
Data Distribution Using an Infinite Sample-and-Hold	578
Section 8-3: Digital Potentiometers	581
Modern Digital Potentiometers in Tiny Packages	582
Digital Potentiometers with Nonvolatile Memory	584
One-Time Programmable (OTP) Digital Potentiometers	585
Digital Potentiometer AC Considerations	586
Application Examples	587
Section 8-4: Digital Audio	591
Sampling Rate and THD + N Requirements for Digital Audio.....	592
Overall Trends in Digital Audio ADCs and DACs	595
Voiceband Codecs.....	596
High Performance Audio ADCs and DACs in Separate Packages	597
High Performance Multichannel Audio Codecs and DACs	600
Sample Rate Converters	602
Section 8-5: Digital Video and Display Electronics	607
Digital Video.....	607
Digital Video Formats	608
Serial Data Interfaces	612
Digital Video ADCs and DACs: Decoders, and Encoders	612
Specifications for Video Decoders and Encoders.....	614
Display Electronics.....	615
Flat Panel Display Electronics	619

Contents

CCD Imaging Electronics	622
Touchscreen Digitizers	627
Section 8-6: Software Radio and IF Sampling	633
Evolution of Software Radio	634
A Receiver Using Digital Processing at Baseband.....	635
Narrowband IF-Sampling Digital Receivers	636
Wideband IF-Sampling Digital Receivers.....	639
Increasing ADC Dynamic Range Using Dither.....	649
Wideband Radio Transmitter Considerations.....	655
Cellular Telephone Handsets	659
The Role of ADCs and DACs in Cellular Telephone Handsets.....	661
SoftFone® and Othello Radio Chipsets from Analog Devices	662
Time-Interleaved IF Sampling ADCs with Digital Post-Processors	667
Advanced Digital Post Processing.....	671
Advanced Filter Bank (AFB)	672
AFB Design Example: The AD12400 12-Bit, 400 MSPS ADC	673
Section 8-7: Direct Digital Synthesis (DDS).....	677
Introduction to DDS	677
Aliasing in DDS Systems	681
Frequency Planning in DDS Systems.....	682
Modern Integrated DDS Systems	684
Section 8-8: Precision Analog Microcontrollers	693
Characteristics of the MicroConverter Product Family	694
Some Σ-Δ MicroConverter Applications	700
ADuC7xxx MicroConverter Products Based on the ARM7 Processor Core	702
Chapter 9: Hardware Design Techniques.....	709
Section 9-1: Passive Components	711
Capacitors	711
Dielectric Absorption	712
Capacitor Parasitics and Dissipation Factor	714
Tolerance, Temperature, and Other Effects	715
Assemble Critical Components Last	715
Resistors and Potentiometers.....	718
Resistor Parasitics.....	720
Thermoelectric Effects	720
Voltage Sensitivity, Failure Mechanisms, and Aging	722
Resistor Excess Noise	723
Potentiometers	723
Inductance.....	725
Stray Inductance	725
Mutual Inductance.....	725
Ringing	728
Parasitic Effects in Inductors.....	728
Q or “Quality Factor”	729
Don’t Overlook Anything.....	729

Section 9-2: PC Board Design Issues	733
Resistance of Conductors	733
Voltage Drop in Signal Leads—“Kelvin” Feedback	735
Signal Return Currents	736
Grounding in Mixed Analog/Digital Systems	737
Ground and Power Planes	738
Double-Sided versus Multilayer Printed Circuit Boards.....	739
Multicard Mixed-Signal Systems.....	740
Separating Analog and Digital Grounds.....	740
Grounding and Decoupling Mixed-Signal ICs with Low Digital Currents	742
Treat the ADC Digital Outputs with Care	743
Sampling Clock Considerations	744
The Origins of the Confusion about Mixed-Signal Grounding: Applying Single-Card Grounding Concepts to Multicard Systems	746
Summary: Grounding Mixed-Signal Devices with Low Digital Currents in a Multicard System	747
Summary: Grounding Mixed-Signal Devices with High Digital Currents in a Multicard System	748
Grounding DSPs with Internal Phase-Locked Loops.....	748
Grounding Summary	749
Some General PC Board Layout Guidelines for Mixed-Signal Systems	750
Skin Effect.....	751
Transmission Lines.....	753
Be Careful With Ground Plane Breaks.....	753
Ground Isolation Techniques.....	754
Static PCB Effects	756
Sample MINIDIP and SOIC Op Amp PCB Guard Layouts	758
Dynamic PCB Effects	760
Stray Capacitance	761
Capacitive Noise and Faraday Shields	762
The Floating Shield Problem.....	762
Buffering ADCs Against Logic Noise	763
Section 9-3: Analog Power Systems.....	767
Linear IC Regulation	768
Some Linear Voltage Regulator Basics	768
Pass Devices	770
±15 V Regulator Using Adjustable Voltage ICs	770
Low Dropout Regulator Architectures	771
Fixed-Voltage, 50/100/200/500/1000/1500 mA LDO Regulators	772
Adjustable Voltage, 200 mA LDO Regulator.....	774
Charge-Pump Voltage Converters	775
Regulated Output Charge-Pump Voltage Converters	776
Linear Post Regulator for Switching Supplies	778
Grounding Linear and Switching Regulators	779
Power Supply Noise Reduction and Filtering	782
Capacitors.....	782

Contents

Ferrites.....	786
Card Entry Filter.....	787
Rail Bypass/Distribution Filter.....	788
Local High Frequency Bypass/Decoupling.....	789
Section 9-4: Overvoltage Protection	793
In-Circuit Overvoltage Protection	793
General Input Common Mode Limitations	793
Clamping Diode Leakage	795
A Flexible Voltage Follower Protection Circuit	796
Common-Mode Overvoltage Protection Using CMOS Channel Protectors	797
CM Overvoltage Protection Using High CM Voltage In Amp	798
Inverting Mode Op Amp Protection Schemes	800
Amplifier Output Voltage Phase-Reversal	800
An Output Phase-Reversal Do-it-Yourself Test.....	802
Fixes for Output Phase-Reversal	802
Input Differential Protection	803
Protecting In Amps Against Overvoltage	804
Overvoltage Protection Using CMOS Channel Protectors.....	808
Digital Isolators	810
Out-of-Circuit Overvoltage Protection	813
ESD Models and Testing	817
Section 9-5: Thermal Management.....	823
Thermal Basics	823
Heat Sinking	825
Data Converter Thermal Considerations	829
Section 9-6: EMI/RFI Considerations	833
EMI/RFI Mechanisms	834
EMI Noise Sources.....	834
EMI Coupling Paths	834
Noise Coupling Mechanisms.....	834
Reducing Common-Impedance Noise.....	835
Noise Induced by Near-Field Interference	836
Reducing Capacitance-Coupled Noise	836
Reducing Magnetically-Coupled Noise	837
Passive Components: Your Arsenal Against EMI	838
Reducing System Susceptibility to EMI.....	839
A Review of Shielding Concepts.....	839
General Points on Cables and Shields	842
Input-Stage RFI Rectification Sensitivity	846
Background: Op Amp and In Amp RFI Rectification Sensitivity Tests	846
An Analytical Approach: BJT RFI Rectification.....	847
An Analytical Approach: FET RFI Rectification	848
Reducing RFI Rectification Within Op amp and In Amp Circuits.....	849
Op Amp Inputs	849
In Amp Inputs	850
Amplifier Outputs and EMI/RFI	852

Printed Circuit Board Design for EMI/RFI Protection.....	852
Choose Logic Devices Carefully	853
Design PCBs Thoughtfully.....	853
Designing Controlled Impedances Traces on PCBs	854
Microstrip PCB Transmission Lines	855
Some Microstrip Guidelines.....	855
Symmetric Stripline PCB Transmission Lines	856
Some Pros and Cons of Embedding Traces.....	857
Dealing with High-Speed Logic	858
Section 9-7: Low Voltage Logic Interfacing	867
Voltage Tolerance and Voltage Compliance	870
Interfacing 5 V Systems to 3.3 V Systems using NMOS FET “Bus Switches”	871
3.3 V/2.5 V Interfaces.....	873
3.3 V/2.5 V, 3.3 V/1.8 V, 2.5 V/1.8 V Interfaces	874
Hot Swap and Hot Plug Applications of Bus Switches	878
Internally Created Voltage Tolerance / Compliance	879
Section 9-8: Breadboarding and Prototyping	881
“Deadbug” Prototyping	882
Solder-Mount Prototyping.....	884
Milled PCB Prototyping.....	885
Beware of Sockets	886
Some Additional Prototyping Points	887
Evaluation Boards.....	887
General-Purpose Op Amp Evaluation Board from the Mid-1990s	888
Dedicated Op Amp Evaluation Boards	888
Data Converter Evaluation Boards	890
Index.....	895